

AMENDMENTS TO THE CLAIMS

Claim 1 (Original) A signal processing apparatus, comprising:

a channel pooling signal processor, including:

a plurality of computation units;

a test interface for testing the function of said plurality of computation units;

a general purpose microprocessor for managing data flow into and out of said channel pooling signal processor; and

an interconnect mechanism for connecting said plurality of computation units, said test interface, and said general purpose microprocessor; and

a digital signal processor connected to said channel pooling signal processor;

wherein said channel pooling signal processor performs more computationally intensive signal processing operations and said digital signal processor performs less computationally intensive signal processing operations.

*b1*  
*A2*

Claim 2 (Original) The signal processing apparatus of Claim 1, wherein a computation unit of said plurality of computation units comprises:

a data sequencer for controlling program execution;

a configurable logic unit; and

a dedicated memory.

Claim 3 (Original) The signal processing apparatus of Claim 1, further comprising:

a second channel pooling signal processor for processing multiple data streams of voice and data information.

*B1*  
*Applicant*

Claim 4 (Original) The signal processing apparatus of Claim 1, wherein said plurality of computation units are heterogenous computation units.

Claim 5 (Original) The signal processing apparatus of Claim 1, wherein said plurality of computation units are homogeneous computation units.

Claim 6 (Original) A method for signal processing, comprising the steps of:  
processing high complexity algorithms in a channel pooling signal processor, said channel pooling signal processor including:  
a plurality of computation units;  
a test interface for testing the function of said plurality of computation units;  
a general purpose microprocessor for managing data flow into and out of said channel pooling signal processor; and  
an interconnect mechanism for connecting said plurality of computation units, said test interface, and said general purpose microprocessor; and  
processing low complexity algorithms in a digital signal processor connected to said channel pooling signal processor.

Claim 7 (Original) The method of Claim 6, further comprising the steps of:

controlling program execution in a computation unit of said plurality of computation units;  
configuring a configurable logic unit in said computation unit in accordance with a standard;

and

storing program execution instructions in a dedicated memory in said computation unit.

*B7 Cont*  
*Agg*  
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Claim 8 (Original) The method of Claim 6, further comprising the steps of:

processing multiple data streams of voice and data information in a second channel pooling signal processor.

Claim 9 (New) A base station transceiver comprising:

an antenna for receiving communication signals; and

a signal processing apparatus having:

a channel pooling signal processor, including:

a plurality of computation units;

a test interface for testing the function of said plurality of computation units;

a general purpose microprocessor for managing data flow into and out of said channel pooling signal processor; and

an interconnect mechanism for connecting said plurality of computation units, said test interface, and said general purpose microprocessor; and

a digital signal processor connected to said channel pooling signal processor;

wherein said channel pooling signal processor performs more computationally intensive signal processing operations and said digital signal processor performs less computationally intensive signal processing operations.

Claim 10 (New) A method for processing communication signals, comprising the steps of:

receiving communication signals;

processing high complexity algorithms on the received communications signals in a channel pooling signal processor, said channel pooling signal processor including:

a plurality of computation units;

a test interface for testing the function of said plurality of computation units;

a general purpose microprocessor for managing data flow into and out of said channel pooling signal processor; and

an interconnect mechanism for connecting said plurality of computation units, said test interface, and said general purpose microprocessor; and

processing low complexity algorithms in a digital signal processor connected to said channel pooling signal processor.